REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 7-13 and 20-27 are allowable and that claims 15-17 would be allowed if written independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-4, 14, 18, 19, and 28-31 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,991,833 ("Wandler") in view of U.S. Pat. No. 6,684,278 ("Sakugawa") and Klein. This is a new ground of rejection. Claims 5, 6, 32, and 33 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Wandler in view of Sakugawa and Klein as applied to claim 1 and claim 28 above and further in view of U.S. Pat. No. 5,845,329 ("Onishi").

Klein is directed to a computer system architecture in which an integrated system controller, such as a northbridge, includes an interrupt request controller, a direct memory access controller and a timer counter unit all integrated within the northbridge. Klein also teaches separate integrated circuits for a processor, south bridge and other circuits. Accordingly, it appears that Klein merely teaches a conventional non integrated system in which the northbridge includes additional circuitry.

Applicants respectfully submit that the Wandler reference should not be viewed in light of the Sakugawa and the Klein reference to obviate Applicants' claims. Sakugawa's invention is aimed at minimizing a microcomputer's power consumption by sacrificing a central processing unit's productivity. (Col. 2, L. 16-21.) Sakugawa uses the access control of a built-in memory 4 to control a central processing unit's power consumption. (Col. 5, L. 57-60.) Sakugawa's memory controller 2 forces a waiting state during a memory access such that a central processing unit is actuated at a low speed, thereby reducing a microcomputer's power consumption. (*Id.*)

Sakugawa even goes a step further by suggesting that the memory controller 2 may stop the clock of the central processing unit 1. (Col. 6, L. 21-34.) This is at odds with Applicants' claims.

Applicants' claimed methods, for example, eliminate a need for converting between bus protocols, which eliminates the need for, among other things, some drivers and interfaces between the central processing unit and northbridge. Applicants' claimed methods allow both a central processing unit and memory to operate at their nominal, specified rates without being slowed down by other components of the system. However, Sakugawa teaches a method for slowing down a processor by having a memory controller intentionally create a bottleneck so that the central processing unit in a microcomputer can conserve power. The Applicants respectfully submit that since their invention is aimed at increasing the efficient, maximum use of a central processing unit, one of ordinary skill in the art would not look to a reference that slows down a central processing unit to solve the problem addressed by Applicants' invention.

The office action alleges that it would have been obvious to one of ordinary skill in the art to use Sakugawa in Wandler for processing the request at a memory rate as claimed because the use of Sakugawa could provide Wandler the ability to adapt to a diversity of memory bandwidths at a given cycle. However, Applicants' claims are not directed to cycle based bandwidth diversity – as such this motivation is not understood and is improper. Moreover, Sakugawa is aimed at minimizing a microcomputer's power consumption by sacrificing a central processing units productivity as noted above. Sakugawa's memory controller forces the waiting state during a memory access so that the central processing unit is controlled at a low speed thereby reducing the microcomputer's power consumption. As such, Sakugawa teaches a method for slowing down a processor by having a memory controller intentionally create a bottle

neck so that the central processing unit in a microcomputer can conserve power. This is at odds with Wandler and with Applicants claimed invention.

For example, Applicants' methods and apparatus are aimed at increasing the efficient, maximum use of a central processing unit and as claimed, have an integrated central processing unit and northbridge on a single substrate and provide memory access requests from a central processing unit to the integrated northbridge at a rate of the central processing unit via an internal bus, by buffering in the northbridge the memory access requests and process, by the northbridge, the memory access requests at a rate of memory thereby allowing the central processing unit to operate at an efficient rate as well as accessing memory at an efficient rate. Sakugawa teaches a different approach and would modify the fundamental operation of Wandler. The proposed combination would simply be a system like that of Sakugawa which effectively bottle necks the operation of a microcontroller and effectively slows the microcontroller down. Neither Wandler nor Applicants' claimed invention are directed to such an operation.

Applicants also respectfully submit that it is improper to parse claim language in such a way as to avoid claim limitations. For example, Applicants claim, among other things, a central processing unit that is integrated with a northbridge on a single substrate wherein the central processing unit is directly coupled to the northbridge via an internal bus having a bus protocol that is a native bus protocol the central processing unit. Klein has been cited for teaching a system that includes a bus that uses native protocol to a CPU. However, this is not what Applicants claim. Applicants claim an integrated central processing unit and northbridge that are coupled via an internal bus that has a bus protocol that is a native bus protocol a central processing unit. Klein teaches a very different structure. For example, Klein specifically teaches separating the CPU from the northbridge as shown and described with reference to Figure 4

(cited by the Examiner). As such, there is no internal bus between an integrated central processing unit and a northbridge in Klein that has a bus protocol that is a native bus protocol of the central processing unit since both the central processing unit and the northbridge in Klein are not integrated but in fact are separate circuits. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

In any event, even construing the teachings of the references as suggested, the resulting system, as best understood, would still be a system employing a central processing unit integrated in the northbridge as taught by Wandler with a memory controller that slows down the central processing unit of Wandler as taught by Sakugawa. In contrast, Applicants claim a method for integrating a personal computing system that includes, among other things, "integrating a central processing unit with a northbridge on to a single substrate such that the central processing unit is directly coupled to the northbridge via an internal bus having a bus protocol that is a native bus protocol of the central processing unit" and "providing memory access requests from the central processing unit to the northbridge at a rate of the central processing unit via the internal bus."

As to claim 2, Applicants also respectfully request reconsideration as it appears that claim language may have been misapprehended. Wandler has been cited as teaching buffering, in the northbridge, memory access requests from a south bridge that is also integrated on the substrate with the central processing unit in the northbridge and then processing by the northbridge memory access requests from the integrated south bridge at the rate of memory. In order for the claim to be obviated, the cited reference much teach the claim subject matter alleged in the office action. However, Applicants are unable to find any mention of the integration of the south bridge taught in Wandler. Moreover, Applicants are unable to find any teaching of processing

by the northbridge, memory access from an integrated south bridge at the rate of memory. The office action cites column 12 lines 1-13, column 13 lines 26-43, Figure 2 as well as apparently column 6 lines 5-7. However, column 6 lines 5-7 is silent as to any integration of the south bridge into an integrated circuit with a CPU and northbridge or the processing of memory access requests from the integrated south bridge at the rate of memory. In fact, it appears that the Wandler reference teaches an opposite approach, namely, a separate south bridge from the integrated northbridge.

Also as to claim 2, Wandler is cited as integrating a south bridge onto the same substrate as a central processing unit and a northbridge. (Citing to Fig. 2; Col. 6. Lines 5-7.) However, Figure 2 shows a south bridge 100, northbridge 50, and central processing unit 25 in a computer system 10 having, among other things, a display 62, not a single substrate. (Col. 5, L. 66.) Applicants make similar suggestions regarding the rejections of claim 3 for memory and claim 4 for a graphics controller. As such, these claims are also in condition for allowance.

As to claim 14, Applicants respectfully reassert the relevant remarks made above. For example, the Office Action cites [10] (in Wandler) as the claimed substrate containing both the memory and the northbridge. However, [10] is a computer system 10 with a display 62, not a single substrate. Therefore, Wandler does not teach the claimed structure.

The dependent claims all depend on allowable base claims, add additional novel and nonobvious subject matter, and are believed to be in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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